

2 P | a charge donor layer comprised of a first Group III-V
3 material; [and] *ry*

4 P | a channel layer disposed adjacent said charge donor
5 layer and comprised of a second Group III-V material having
6 a bandgap energy lower than the bandgap energy of said first
7 Group III-V material; *ry*

8 P | a pair of ohmic contacts disposed over first portions
9 of said charge donor and channel layers and a Schottky
10 barrier contact disposed over second portions of said charge
11 donor and channel layers; and

12 P | means for shielding at least one of said charge donor
13 and channel layers from the effects of surface charges which
14 are present in regions between gate and drain electrodes of
15 the [transistor.] transistor, said means further comprising:

16 P | a first charge screen layer corresponding to a portion
17 of said charge donor layer; and

18 P | a second charge screen layer comprised of a third Group
19 III-V material having a bandgap energy lower than the
20 bandgap energy of said first Group III-V material disposed
21 adjacent said gate electrode and at least one drain and
22 source electrodes of said transistor.

1 2. (Amended) The [structure,] transistor, as recited
2 in claim 1, wherein [said shielding means includes a portion
3 of] said charge donor layer has [with] a first portion

4 adjacent said channel being of an undoped Group III-V
5 material, an intermediate [a immediate] portion adjacent said
6 undoped portion comprised of a dopant sheet of N-type dopant
7 having a concentration of dopant atoms confined to a few
8 atomic layer thicknesses of the charge donor layer and a
9 third portion of said layer being a relatively lightly doped
10 region of said charge donor layer with said third portion
11 corresponding to the first charge screen layer.

1 (A) 3. (Amended) The transistor, as recited in claim
2 [1,] wherein said second [shielding means comprises a pair
3 of] charge screen layer [layers] comprised of relatively
4 lightly doped Group III-V material has a dopant
5 concentration of 1×10^{17} to 5×10^{17} atoms/cc in a region
6 thereof [materials] disposed adjacent the gate electrode,
7 and source and drain electrodes of the [high electron
8 mobility] transistor.

1 4. (Amended) The [high electron mobility] transistor,
2 as recited in claim 3, wherein said [shielding means further
3 comprises a recess having a first width disposed through
4 the] first charge screen layer has a first recess having a
5 first width disposed therethrough and a second recess
6 aligned over the first recess having a second, substantially
7 larger width than that of the first recess disposed through

8 a portion of the thickness of the [first charge screen layer
9 and the] second charge screen layer.

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1 5. (Amended) A high electron mobility transistor
2 comprises:

3 a semi-insulating substrate;

4 a channel layer comprised of a first Group III-V
5 material disposed over said semi-insulating substrate;

6 a charge donor layer disposed over said channel layer
7 and [region] comprised of a second Group III-V material
8 having a bandgap higher than that of the corresponding
9 bandgap of the material of the channel layer, a first region
10 of said second [undoped] Group III-V material being undoped,
11 [u]having a bandgap higher than the corresponding bandgap of
12 the channel layer,] a second region of said charge donor
13 layer having a dopant [profile] confined to a few angstroms
14 thickness of said charge donor layer and having a dopant
15 concentration generally in the range of about 2.0×10^{12} to
16 5×10^{12} atoms per square centimeter, [said charge donor layer
17 having] and a third region comprised of a relatively lightly
18 doped portion of said second Group III-V material;

19 a charge screen layer comprised of a lightly doped N-
20 type region of a second [the first] Group III-V material
21 disposed over said third region of said charge donor layer;

22 a pair of spaced contact regions comprised of said
B 23 ~~second~~ [first] Group III-V material having a dopant
24 concentration greater than about 1×10^{18} [a/cc] atoms per
25 cubic centimeter disposed over said charge screen layer;
26 a gate electrode disposed in Schottky barrier contact
27 with said third ~~portion~~^{region} of said charge donor layer; and
28 a pair of source and drain electrodes disposed in ohmic
29 contact with said spaced contact ~~layers~~^{regions}.

1 6. (Amended) The transistor, [structure,] as recited
2 in Claim 5, wherein [said gate electrode is disposed within
3 a first aperture provided in] said third ~~portion~~^{region} of said
4 charge donor layer and a selective portion of said charge
5 screen layer has a first aperture and wherein said charge
6 screen layer and spaced contact ~~layers~~^{regions} [layer] have therein
7 a second relatively wide aperture compared to that of the
8 first aperture and said second aperture disposed in
9 alignment over the first aperture and said gate is disposed
10 in said first aperture.

Please add the following Claims 7-16.

1 5. The transistor, as recited in Claim 1, wherein
2 said charge donor layer is comprised of aluminum gallium
3 arsenide and said channel layer is comprised of gallium
4 arsenide.

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6. The structure, as recited in claim 1, wherein said
first material is aluminum gallium arsenide, said second
material is indium gallium arsenide, and said third material
is gallium arsenide.

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7. The transistor, as recited in claim 1, wherein
said charge donor layer is a first charge donor layer and
said transistor further comprises a second charge donor
layer comprised of said first Group III-V material disposed
on an opposing surface of said channel layer such that said
first charge donor layer and said second charge donor layer
are disposed to sandwich said channel layer.

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8. The transistor, as recited in claim 7, wherein
said second charge donor layer comprises:

14. a first portion adjacent said channel layer being of an
undoped first Group III-V material, an intermediate portion
of said charge donor layer adjacent said undoped portion
comprised of a dopant sheet of n-type dopant having a
concentration of dopant atoms confined to a few atomic layer
thicknesses of the second charge donor layer and a third
portion of said second charge donor layer disposed adjacent
said dopant sheet being a relatively lightly doped region of
said first Group III-V material.

1 11. The transistor, as recited in claim 10, wherein
2 said first charge donor layer has a first portion adjacent
3 said channel being of an undoped first Group III-V material,
4 an intermediate portion of said charge donor layer adjacent
5 said undoped portion comprised of a dopant sheet of n-type
6 dopant having a concentration of dopant atoms confined to a
7 few atomic layer thicknesses of the first charge donor
8 layer, and a third portion of said first charge donor layer
9 being a relatively lightly doped region of said first charge
10 donor layer with said third portion corresponding to the
11 first charge screen layer.

1 12. The transistor, as recited in claim 9, wherein
2 said second charge screen layer is comprised of doped third
3 Group III-V material disposed adjacent the gate electrode
4 and source and drain electrodes of the high electron
5 mobility transistor and having a dopant concentration in the
6 range of about 1×10^{17} to 5×10^{17} atoms/cc.
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1 11 13. The transistor, as recited in claim 12, wherein
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3 said first charge screen layer has a first recess having a
4 first width disposed therethrough and a second recess
5 aligned over the first recess having a second, substantially
 larger width than that of the first recess and disposed

6 through a portion of the thickness of the second charge
7 screen layer.

1 14. A high electron mobility transistor comprising:
2 a substrate;
3 a channel layer comprised of a first Group III-V
4 material disposed over said substrate;
5 a charge donor layer disposed over said channel layer
6 comprised of:
7 a first region of undoped second Group III-V
8 material having a bandgap higher than the corresponding
9 bandgap of the material of the channel layer;
10 a second region of said charge donor layer having
11 a dopant confined to a few angstroms thickness of said
12 charge donor layer and having a dopant concentration in
13 the range of about 2×10^{12} to 5×10^{12} atoms per square
14 centimeter; and
15 a third region comprised of a relatively lightly
16 doped portion of said second Group III-V material
17 compared to the dopant concentration of said second
18 region;
19 a charge screen layer comprised of a third Group III-V
20 material disposed over said third region of said charge
21 donor layer with said charge screen layer having a portion
22 of lightly doped n-type material;

23 a gate electrode disposed in Schottky barrier contact
B 24 with said third ^{region}_{portion} of said charge donor layer in a
25 region of said charge donor layer underlying the portion of
26 said charge screen layer which is lightly doped n-type; and
27 a pair of source and drain electrodes disposed in ohmic
28 contact over said charge screen layer.

1 15. The transistor, as recited in Claim 14, further
2 comprising, a pair of spaced contact regions comprised of
3 ^{third}_{first} Group III-V material having a dopant
4 concentration greater than about 1×10^{18} atoms per square
5 centimeter disposed between said corresponding pair of
6 source and drain electrodes and said charge screen layer.

1 16. The structure, as recited in claim 14, wherein
2 said charge donor layer is comprised of aluminum gallium
3 arsenide and said channel layer is comprised of gallium
4 arsenide.

1 17. The structure, as recited in claim 14, wherein
2 said first material is indium gallium arsenide, said second
3 material is aluminum gallium arsenide, and said third
4 material is gallium arsenide.

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